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09/706,154	11/03/2000	Marlo Nemirovsky	P3816	5008

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/706,154	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 6-11 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani (patent No. 5,669,537) in view of Sollars (patent No. 5,900,025) .

3. Sharangpani taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Instruction cache (206k,304) (e.g., see figs. 2,3) (on chip memory or external memory subsystem in fig. 4) (e.g., see col.4, line 63-col. 5, line 40);

b) Fetch logic (302,402) coupled to the instruction cache enabled to concurrently fetch instructions from the instruction cache (e.g., see figs. 3,4, and col. 5, line 21-col. 7, line 61);

c) A plurality of instruction queues 322,415,416,417,418) coupled the said fetch logic where each one of said plurality of instruction queues is associated with at least one instruction stream (e.g., see fig. 4);

d) dispatch stage coupled to said plurality of instruction queues for selecting and dispatching instructions for said an instruction stream to a set of execution units[the instruction queue is part of the dispatch stage in fig. 4 of Sharangpani and used for

dispatch of instructions by the dispatch stage and consequently would inherently be coupled to the instruction queues] (e.g., see col. 6, lines 28-64).

4. Sharangpani did not expressly detail (claims 1,7) that the instructions that were fetched concurrently were for a plurality of threads and the queue were for a plurality of threads. Sollars however taught concurrently fetching instructions from plural threads from cache(16) to a plurality of queues (254a-254d)(e.g., see fig. 15) and selecting instructions from the queue using selector (256) and sending the instructions to the execution units (e.g., see fig. 15)(e.g., see col. 2, line 15-col. 3, line 10 and col. 6, lines 16-35 and col. 14, lines 1-40).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Sharangpani and Sollars. Both references were directed toward the problems of fetching and providing instructions to plural execution units in parallel. One of ordinary skill would have been motivated to incorporate the Sollars teachings of fetching instructions for plural threads to plurality of queues and then selecting queue for dispatch to execution units at least to reduce the time needed to fetch instructions to execution units and effectively decoupling the fetch of instructions from the dispatch of instructions to execution units (e.g., see col. 14, lines 25-36).

6. Sharangpani did not expressly detail (claims 1,7) select logic coupled to the instruction cache for selecting ones of the plurality of streams to fetch instructions from the instruction cache. Sharangpani, however, taught fetching instructions from cache that are steered to plural distinct queues, each queue for providing instruction to a particular distinct type of execution unit (e.g., see fig. 4) From this the fetch unit fetches

the instruction for a different type of execution units. Also, Sharagpani taught branch execution logic and branch prediction logic for fetching instructions from cache (e.g., see fig. 4) the branch micro-pipeline is taught as affecting the operation of the execution front end in fetching and execution instructions down the correct path of the branch. Therefore it would have been obvious to one of ordinary skill that in at least one implementation of the Sharangpani teachings the system comprised select logic coupled to the instruction cache for selecting one of the plurality of instruction streams to fetch instructions from the instructions cache. This is apparent also because since the fetching is for plural streams and selection of instructions for each stream would have been required. Further (as to claims 1,2,4,7,8). One of ordinary skill would have been motivated to provide for the selection of streams to fetch so that if one stream did not have any more instructions in the cache then the system would not waste time trying to receive fetch requests from the stream that had no further instructions in the cache although it may have instructions in its queue. In this case the number of streams being fetched would have been less than the number of instruction streams executing. On the other hand, Sollars taught fetching of plural streams to queues(up to eight) from cache where some streams were active and some were inactive and the selection of queues for sending instructions to execution units [this provides for the number of streams being fetched being less than the number of queued streams (e.g.,see fig. 15 of Sollars)].

7. This Sollars teaching of storing of instructions for separate thread in separate queues where some threads are active and some are inactive as discussed above

provides for the number of streams or threads fetched (i.e., only active threads) being less than the number of queues.

8. Claims 1 and 7,13,14 and 15 comprise monitoring of the queues and selecting of streams to fetch from the instruction cache based on the monitoring. Sollars taught plural instruction queues that are selected to receive instructions from cache and the output instructions are selected to be sent to execution unit (e.g., see fig. 15 of Sollars). Sollars taught that some streams were active and some inactive (as discussed above). Sollars taught the operation of monitoring other queues in the system namely the request queues to determine if it was empty (e.g., see col. 12, lines 42-58). Consequently one of ordinary skill would have been motivated to monitor queues used in the Sollars system for determining actions to be taken regarding the queued data or instructions. Further since when a queue was not empty more instructions would have been waiting to be executed and when the queue was full no more instructions could have been fetched to the queue without losing and instruction then monitoring the queues would have been obvious to one of ordinary skill at least to ensure that all instructions queued were executed and there was room in a queue when an instruction was fetched to the queue. Also since the Sollars queue stored instructions for separate streams then clearly when one queue for a stream was full then one of ordinary skill would have been motivated to select another stream. This operation provides for the fetching of threads based on monitoring.

9. As to the number of instruction queues (claim 16) Sollars taught the use of four or eight instruction queues (e.g., see col. 14, lines 25-36). Also the use caches with

multiple ports less than four ports such as two port cache was well known in the art at the time of the claimed invention. One of ordinary skill would have been motivated to use a two or three port cache as the cost for implementation would have been less than a four or more port cache. Also the use of a cache with two or three ports would have allowed simultaneous access to the cache facilitating the fetching of instruction in the Sollars system to the queues.

10. As to the limitation of claim 17, since Sollars taught selecting of queues for sending data to the execution units in fig 15. Clearly some execution units dispatched instructions while other execution units did not on a per cycle basis. Therefore clearly the number of instructions from each queue dispatched was variable.

11. As per claims 3,9,10,Since Sharanpani and Sollars systems execute plural streams at the same time plural program counters would have been required to keep track of where each stream the execution unit were executing so that the correct next instruction could be fetched (e.g., see fig. 3, of Sharangpani; and figs. 5,6 and col. 8, lines 43-50 of Sollars where PC element 112a and 113a store the current address being executed or program counter (see col. 9, lines 9-27) is part of the thread control register set).

12. As per claim 6, Sharangpani taught the fetch logic concurrently storing instructions into one of said plurality of instruction queues that would be associated in the combined system with said ones of said plurality of instruction streams by said fetch logic (e.g., see fig. 4 and col. 8, line 12-col. 9, line 56).

13. As per claim 11, Sharangpani taught dispatching stage logic dispatching instructions to a plurality of execution units (e.g., see fig. 4 and col. 6, lines 36-66).

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani and Sollars as applied to claims 1-4,6-11,13-17 above, and further in view of Hirata (patent No. 5,430,851).

15. As per claim 12, Sharangpani did not expressly detail the plurality of execution units comprises eight arithmetic logic units (ALUs) and two memory units. Hirata taught eight units comprising two load store units an six functional unit (e.g., see fig. 2a). The implementation in the embodiment detailed by Sharangpani using four execution units would not have prevented modification in the implementation of the Sharangpani teachings by expansion of the system to incorporate any reasonable number of execution units. The particular number of execution units in the range of ten would not be beyond the level of skill of one of ordinary skill to implement using the teachings of Sharangpani and Hirata Further the connection to memory unit especially since the Sharangpani system comprised load/store unit would have been within the level of skill of one of ordinary skill in the art considering the Sharangpani teachings to implement. The motivation to implement the system in that manner comes from the applications that would be implemented and the Examiner contends that an application for processing multiple streams of search queries such as via as would be used in a search engine would have motivated one of ordinary skill to expand the Sharangpani system to incorporate ten processors or two memories.

16. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Sharangpani and Hirata. Both references were directed toward the problems of fetching and providing instructions to plural execution units in parallel. One of ordinary skill in the art would have been motivated to incorporate the Hirata teachings of expanding the number of execution units to eight and incorporating two load store units at least to provide the functionality to implement multiple streams for search query applications.

Response to Arguments

Applicant's arguments with respect to claims 1-4,6-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The change in scope of the amended claims has necessitated a new search.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER